

Amendment and Response

Applicant: Junghwon Suh

Serial No.: 10/757,275

Filed: Jan. 14, 2004

Docket No.: 200353931US

Title: MEMORY WITH AUTO REFRESH TO DESIGNATED BANKS

REMARKS

The following remarks are made in response to the Office Action mailed May 5, 2004. Claims 1-21 were rejected. Claims 1-21 remain pending in the application and are presented for reconsideration and allowance. Claim 5 has been amended. Claims 22-24 have been added.

Claim Rejections under 35 U.S.C. § 103

Claims 1-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cowles et al., U.S. Patent No. 5,959,929 ("Cowles").

The rejection of claims 1-21 35 under U.S.C. §103(a) as being unpatentable over Cowles should be withdrawn because the rejection fails to establish a case of *prima facie* obviousness. Referring to §706.02(j) of the M.P.E.P., one of the three basic criteria that must be met to establish a *prima facie* case of obviousness is that *the prior art reference must teach or suggest all the claim limitations*. As described below, Cowles does not teach or suggest all of the claims limitations of independent claims 1, 9, or 17 and the claims depending therefrom. Accordingly, Cowles cannot support a case of *prima facie* obviousness over independent claims 1, 9, or 17 and the claims depending therefrom.

Claim 1 recites, *inter alia*:

2ⁿ refresh row address counter circuits each configured to generate a set of refresh row address signals in response to 2ⁿ refresh enable signals;

a multiplexer circuit configured to provide the sets of refresh row address signals to the 2ⁿ DRAM banks in response to the 2ⁿ refresh enable signals; and

...

wherein the 2ⁿ bank enable signals cause at least two but less than all of the 2ⁿ DRAM banks to be refreshed using at least

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two of the sets of refresh row address signals in response to the 2ⁿ refresh enable signals.

Cowles does not teach or suggest “2ⁿ refresh row address counter circuits each configured to generate a set of refresh row address signals in response to 2ⁿ refresh enable signals” as recited in claim 1. As noted by the Office Action, Cowles teaches “a refresh counter 56”. Cowles, Figure 1, col. 5, line 49, and col. 6, line 6. This teaching of a *single* refresh counter does not teach or suggest the “2ⁿ refresh row address counter circuits” recited in claim 1 and further does not teach or suggest that each counter circuit is “configured to generate a set of refresh row address signals in response to 2ⁿ refresh enable signals”.

In addition, Cowles does not teach or suggest “a multiplexer circuit *configured to provide the sets of refresh row address signals to the 2ⁿ DRAM banks* in response to the 2ⁿ refresh enable signals” as recited in claim 1 (emphasis added). Although Cowles may teach providing a *single* set of address signals from refresh counter to row address mux 36 in Figure 1, Cowles does not teach or suggest that mux 36 provides *multiple* sets of address signals to memory banks 22, 24, 26, and 28.

Further, Cowles does not teach or suggest “wherein the 2ⁿ bank enable signals cause at least two but less than all of the 2ⁿ DRAM banks to be refreshed using at least two of the sets of refresh row address signals in response to the 2ⁿ refresh enable signals” as recited in claim 1. Because Cowles does not teach or suggest the features of claim 1 noted above, Cowles does not teach or suggest refreshing “at least two but less than all of the 2ⁿ DRAM banks . . . using at least two of the sets of refresh row address signals” as recited in claim 1.

Because Cowles does not teach or suggest the features of claim 1 noted above, Cowles does not support a *prima facie* case of obviousness over claim 1. Accordingly, Applicant respectfully requests that the rejection of claim 1 be withdrawn. Claims 2-8 depend from claim 1 and are believed to patentably distinguish over the cited reference for at least the above reasons. Further, Applicant respectfully submits that claims 2-6 and 8 each recite additional features not taught or suggested by Cowles.

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Claim 9 recites, *inter alia*:

a dynamic random access memory (DRAM) comprising:

...

2ⁿ refresh row address counters;

... ; and

a memory controller configured to generate a bank selector value associated with an auto refresh operation and configured to initiate the auto refresh operation to cause at least two of the banks to be refreshed using at least two of the refresh row address counters by providing the bank selector value to the DRAM using the n bank address inputs and at least one of the m row address inputs.

Cowles does not teach or suggest “2ⁿ refresh row address counters” as recited in claim 9. As noted above, Cowles teaches “a refresh counter 56”. Cowles, Figure 1, col. 5, line 49, and col. 6, line 6. This teaching of a *single* refresh counter does not teach or suggest the “2ⁿ refresh row address counters” recited in claim 9.

In addition, Cowles does not teach or suggest “a memory controller ... configured to initiate the auto refresh operation to cause at least two of the banks to be refreshed using at least two of the refresh row address counters by providing the bank selector value to the DRAM using the n bank address inputs and at least one of the m row address inputs” as recited in claim 9. Although Cowles teaches an auto refresh command as cited by the Office Action (col. 5, lines 42-57), the auto refresh command contemplated by Cowles does not “cause at least two of the banks to be refreshed using at least two of the refresh row address counters” as recited in claim 9.

Because Cowles does not teach or suggest the features of claim 9 noted above, Cowles does not support a *prima facie* case of obviousness over claim 9. Accordingly, Applicant

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respectfully requests that the rejection of claim 9 be withdrawn. Claims 10-16 depend from claim 9 and are believed to patentably distinguish over the cited reference for at least the above reasons. Further, Applicant respectfully submits that claims 10-14 and 16 each recite additional features not taught or suggested by Cowles.

Claim 17 recites, *inter alia*:

receiving an auto refresh command;
receiving a bank selector value that designates at least two
but less than all of the banks; and
refreshing the banks designated by the bank selector value.

Cowles does not teach or suggest “receiving a bank selector value that designates at least two but less than all of the banks” and “refreshing the banks designated by the bank selector value” as recited in claim 17. As noted above, Cowles teaches an auto refresh command as cited by the Office Action (col. 5, lines 42-57). Cowles does not teach or suggest, however, “receiving a bank selector value that designates at least two but less than all of the banks” as recited in claim 17. Accordingly, Cowles does not teach or suggest “refreshing the banks designated by the bank selector value” as recited in claim 17.

Because Cowles does not teach or suggest the features of claim 17 noted above, Cowles cannot support a *prima facie* case of obviousness over claim 17. Accordingly, Applicant respectfully requests that the rejection of claim 17 be withdrawn. Claims 18-21 depend from claim 17 and are believed to patentably distinguish over the cited reference for at least the above reasons. Further, Applicant respectfully submits that claims 18-21 each recite additional features not taught or suggested by Cowles.

Claims 22-24 are believed to patentably distinguish over the cited reference for at least the reasons given above for claim 1. Further, Applicant respectfully submits that claims 22-24 each recite additional features not taught or suggested by Cowles.

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CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-24 are not taught or suggested by the cited reference and are in form for allowance. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-24 is respectfully requested.

The Patent Office is hereby authorized to charge Deposit Account No. 50-0471 for any fees due.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Respectfully submitted,

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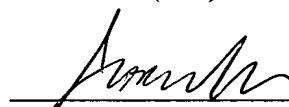
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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 28th day of July, 2004.

By 

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